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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHOUDHURY, AZIZUL Q	
ART UNIT	**PAPER NUMBER**
2145	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/858,323	JUNGCK ET AL.	
	Examiner	Art Unit	
	Azizul Choudhury	2145	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 20 and 37 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Within the claims, the applicant claims the use of "stateless processors." With the well-known understanding in the art that digital designs require the use of states, it is unknown to the examiner how a processor (i.e. microprocessor) is able to be stateless. More details describing the claimed invention are requested for any future amended claims.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The current claims are broad and general to the point of failing to truly detail the functions being performed. One example continues to be the trait within the claims that the data is filtered. However, no details are claimed for what is being filtered, or how the filtering is performed, or what incentives are offered. Another example is the description of processor placement/layout within the design without claiming what incentives such placement/layout offers. It is not well known within the art what results the claimed processor placements will yield. Finally, the claims state that packets are selectively intercepted. No details are claimed regarding how the packets are selected and what process is performed on the selected packets. These three 112 issues noted are simply the most apparent examples. It is strongly believed by the examiner that more detailed claim amendments are required to provide a more accurate design description.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dally et al (US Pat No: US006285679B1) in view of Irwin (US Pat No: US006393026B1), hereafter referred to as Dally in view of Irwin, respectively.

1. With regards to claims 1, 20, 37 and 38, Dally teaches an architecture for intercepting and processing packets transmitted from a source to a destination over a network, the architecture comprising: a packet interceptor coupled with said network and operative to selectively intercept said packets prior to receipt by said destination; at least one primary processor coupled with said packet interceptor and operative to perform stateless processing tasks on said intercepted packets, said at least one primary processor including: at least two stateless packet processors coupled in parallel, said processing of said intercepted packets being distributed among said at least two stateless packet processors; at least one secondary processor coupled with said at least one primary processor and operative to perform stateful processing tasks on said intercepted packets, said at least one secondary processor including: at least two stateful packet processors coupled in series with each other, each of said at least two stateful packet processors operative to perform a portion of said stateful processing tasks on said intercepted packets, a last one in said series of said at least two stateful packet processors being coupled with said network and operative to selectively release said intercepted packet back to said network

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). There exists a network input pathway and a network output pathway (Figure 8, Dally). The line interface circuit handles the input and output of data. Furthermore, the packets are converted from one

format to another while having certain information (header information) extracted (a method of filtering) from it (column 7, lines 1-18, Dally). Hence, data is processed upon and after being received and is sent out for delivery. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

2. With regards to claims 2 and 21, Dally teaches through Irwin the architecture, wherein said network further comprises a bi-directional network having an upstream flow and a downstream flow, said architecture further comprising at least two of said at least one primary processor and at least two of said at least one secondary processor, a first of said at least two primary and secondary processors being coupled with said upstream flow and a second of said at least two primary and secondary processors being coupled with said downstream flow

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor)

(column 2, lines 30-42, Dally). There exists a network input pathway and a network output pathway (Figure 8, Dally). Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

3. With regards to claims 3 and 22, Dally teaches through Irwin the architecture, wherein said at least two secondary processors are capable of sharing state information between each other

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). In addition, Dally discloses that data is shared between processors (column 4, lines 34-35, Dally). Plus, Dally's disclosed design allows for state information to be shared (column 13, lines 29-52, Dally) in multiprocessor designs. The state information is presented in a table that is referred to by each output channel. Since output channel is a separate process,

each is able to have it's own processor. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

4. With regards to claims 4 and 23, Dally teaches through Irwin the architecture, wherein said at least two primary packet processors are coupled together and operative to share data

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). Furthermore, the packets are converted from one format to another while having certain information (header information) extracted from it (column 7, lines 1-18, Dally). Hence, data is processed upon and after being received and is sent out for delivery. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

5. With regards to claims 5 and 24, Dally teaches through Irwin the architecture, wherein said at least two primary packet processors are coupled together with at least one co-processor

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). Furthermore, the packets are converted from one format to another while having certain information (header information) extracted from it (column 7, lines 1-18, Dally). Hence, data is processed upon and after being received and is sent out for delivery. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

6. With regards to claims 6 and 25, Dally teaches through Irwin the architecture, wherein said co-processor comprises a classification co-processor

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). Furthermore, the packets are converted from one format to another while having certain information (header information) extracted from it (column 7, lines 1-18, Dally). Hence, data is processed upon and after being received and is sent out for delivery. Plus, a determination process is made (equivalent to the claimed classification process) by the design for the data packet to be routed to a certain location. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have

combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

7. With regards to claims 7 and 26, Dally teaches through Irwin the architecture, wherein said co-processor comprises a content addressable memory

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). Furthermore, the packets are converted from one format to another while having certain information (header information) extracted from it (column 7, lines 1-18, Dally). Hence, data is processed upon and after being received and is sent out for delivery. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

8. With regards to claims 8 and 27, Dally teaches through Irwin the architecture, wherein said at least two secondary packet processors are coupled with said at least two primary packet processors and operative to share state information

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). In addition, Dally discloses that data is shared between processors (column 4, lines 34-35, Dally). Plus, Dally's disclosed design allows for state information to be shared (column 13, lines 29-52, Dally) in multiprocessor designs. The state information is presented in a table that is referred to by each output channel. Since output channel is a separate process, each is able to have it's own processor. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

9. With regards to claims 9 and 28, Dally teaches through Irwin the architecture, wherein said at least two secondary packet processors and said at least two primary packet processors comprise network processors

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). There exists a network input pathway and a network output pathway (Figure 8, Dally). The line interface circuit handles the input and output of data. Furthermore, the packets are converted from one format to another while having certain information (header information) extracted from it (column 7, lines 1-18, Dally). Then a determination process occurs to properly send out the data. Hence, data is processed after receipt and before delivery of the data packets. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

10. With regards to claims 10 and 29, Dally teaches through Irwin the architecture, wherein said network processor is capable of bi-directional operation and characterized by a bi-directional throughput, said architecture comprising utilizing said network processor uni-directionally wherein said bi-directional throughput is devoted to uni-directional processing

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). There exists a network input pathway and a network output pathway (Figure 8, Dally). The line interface circuit handles the input and output of data. Furthermore, the packets are converted from one format to another while having certain information (header information) extracted from it (column 7, lines 1-18, Dally). Hence, data is processed upon and after being received and is sent out for delivery. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

11. With regards to claims 11 and 30, Dally teaches through Irwin the architecture, wherein said stateless processing tasks comprise filtering said intercepted packets

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). There exists a network input pathway and a network output pathway (Figure 8, Dally). The data packets are converted and certain data is extracted (column 7, lines 1-18, Dally). Hence the data is filtered as claimed. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

12. With regards to claims 12 and 31, Dally teaches through Irwin the architecture, wherein one portion of said stateful processing tasks comprises inspection and

analysis of said intercepted packets and another portion of said stateful processing tasks comprises performing an action on said intercepted packets.

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). There exists a network input pathway and a network output pathway (Figure 8, Dally). The data packets are converted and certain data is extracted (column 7, lines 1-18, Dally). Hence the data is inspected and analyzed as claimed. Furthermore, the data is later sent out to the proper location after a process of determination of destination location is performed on the data. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

13. With regards to claims 13 and 32, Dally teaches through Irwin the architecture, wherein said action comprises at least one or modifying, deleting, storing information about and releasing said intercepted packets

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). There exists a network input pathway and a network output pathway (Figure 8, Dally). The data packets are converted and certain data is extracted (column 7, lines 1-18, Dally). Hence the data is modified (converted) and deleted (extracted) as claimed. Plus, the data packets are stored within the design (routing information concerning the data packets are also stored) before being sent out. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

14. With regards to claims 14 and 33, Dally teaches through Irwin the architecture, wherein said packet interceptor is capable of interfacing with an optical network

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). There exists a network input pathway and a network output pathway (Figure 8, Dally). The data is transmitted using SONET links, which are optical (fiber optics) (column 6, line 61, Dally). Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

15. With regards to claims 15 and 34, Dally teaches through Irwin the architecture, wherein said optical network is characterized by compliance with an OC-48 standard

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor)

(column 2, lines 30-42, Dally). There exists a network input pathway and a network output pathway (Figure 8, Dally). The data is transmitted using SONET links, which are optical (fiber optics) (column 6, line 61, Dally). Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

16. With regards to claims 16 and 35, Dally teaches through Irwin the architecture, wherein said packet interceptor is capable of operating substantially at wire speed

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). There exists a network input pathway and a network output pathway (Figure 8, Dally). The data is transmitted using SONET links, which are optical (fiber optics) (column 6, line 61, Dally). Fiber optics are

substantially faster than wire speeds. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

17. With regards to claims 17 and 36, Dally teaches through Irwin the architecture, wherein said stateless and stateful processing tasks are capable of processing any portion of said intercepted packets

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). The data is processed upon and after being received and is sent out for delivery. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

18. With regards to claim 18, Dally teaches through Irwin the architecture, wherein said packet interceptor is coupled with said network via a router

(Dally discloses a design for an Internet Switch Router. The design receives and outputs data packets (equivalent to the claimed packet interceptor) (column 2, lines 30-42, Dally). There exists a network input pathway and a network output pathway (Figure 8, Dally). The line interface circuit handles the input and output of data. Since the design is placed within a network and handles the transportation of data packets, it is acceptable for the design to be coupled to a router. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet

processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

19. With regards to claim 19, Dally teaches through Irwin the architecture, further comprising a router blade including said packet interceptor, said at least one primary processor and said at least one secondary processor

(Dally discloses a design for an Internet Switch Router. Hence, the design comprises a router as claimed. Dally's disclosure however does not detail the number of processors within the router.

Irwin discloses a design for a router. The router allows for multiple processors (column 3, lines 50-53, Irwin).

Since both Dally and Irwin teach designs with routers, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Dally with those of Irwin, to provide a data packet processing system and method for a router which achieves high processor utilization and has algorithmic flexibility and less data locality problems (column 3, lines 45-49, Irwin)).

Remarks

The amended application received on December 28, 2004 has been carefully reviewed but is not deemed fully persuasive. With regards to the applicant's

representative's remarks concerning the use of multiprocessors in routers, the examiner has now provided an additional art supporting the use of multiple processors in routers. As for the 112 rejections, they have been expanded to clarify the examiner's concerns and add the new concerns over the claimed use of "stateless processors." Finally, the examiner continues to believe that a router is a form of packet interceptor. A router intercepts certain data packets and performs processes on them. Thus, the examiner feels that a router does indeed fit within the claimed design limitations.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Azizul Choudhury whose telephone number is (571) 272-3909. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Valencia Martin-Wallace can be reached on (571) 272-6159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AC

V. Martin Wallace

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